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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NATNAEL, PAULOS M	
ART UNIT	**PAPER NUMBER**
2614	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,382	ZHOU ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-33,39-44 and 54-65* is/are allowed.

6)☒ Claim(s) *1-7,9-11,14,34,45,48,50,51,66,67 and 70* is/are rejected.

7)☒ Claim(s) *8,12,13,35-38,46,47,49,52,53,68 and 69* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1-3, 5, 9-11, 14, 34, 45, 50-51, 66,** are rejected under 35 U.S.C. 102(b) as being anticipated by **Shono**, U.S. Pat. No. **5,436,736**.

Considering claim **1**, Shono discloses all claimed subject matter, note;

a) the claimed a pixel circuit operable to compare a pixel value to a threshold value, is met by Comparator **23**, Fig.4;

b) modify the pixel value, if the pixel value has a predetermined relationship to the threshold value, is met by Adder **22**, fig.4, since the comparator's operation is not a simple addition or summation of the two values; rather, it is a result of a comparison which uses the generated random number as a threshold, i.e., it has or would have some sort of a relationship to pixel value. (see also col. 5, lines 55-65, col. 7, lines 42-44, and col. 8, lines 13-29)

Considering claim **2,** the image processing circuit of claim 1 wherein the pixel value

comprises a luminance pixel value, is inherent because in each pixel the luminance and color difference components would be represented.

Considering claim **3,** the image processing circuit of claim 1 wherein the pixel value comprises a chrominance pixel value.

See rejection of claim 2.

Considering claim **5**, the image processing circuit of claim 1 wherein the compensation value comprises a randomly generated value, is met by the numbers or values generated by the random number generator 24, fig.4;

Considering claim **9**, the image processing circuit of claim 1 wherein the pixel circuit comprises a processor, is inherent in such circuits because without a processor or a controller the circuit would not work properly.

Considering claim **10**, the image processing circuit of claim 1 wherein the pixel circuit is operable to modify the pixel value by adding a compensation value to the pixel value, is met by the adder which adds the binarized BL signal to the pixel signal fH, fig.4;

Considering claim **11**, an image processing circuit, comprising

a) a pixel circuit operable to generate a random number, is met by Random Number Generator 24, Figs.4 and 6;

b) combine the random number with a pixel value, is met by Operator 26', Fig. 6

Considering claim **14**, the claimed image processing circuit of claim 11 wherein the pixel circuit is operable to add the random number to the pixel value, is met by adder 22,Fig.1;

Considering claim **34**, the image processing circuit, wherein the pixel circuit is operable to: generate a first random number, add the first random number to a first pixel value, generate a second random number, and add the second random number to a second pixel value, is met by the random number generator 24 (figs. 4 and 6) which continues to generator random numbers as needed and the adder 22 which would continue to added the pixel number with the output value of the comparator. See also rejection of claims 1 and 11.

Claim **45**, is a method claim of claim 1 and thus, claim 45 is rejected for the same reasons as claim 1;

Considering claim **50**, the method of claim 45 wherein the modifying comprises adding a compensation value to the pixel value, is met by Adder 22, fig.4;

Considering claim **51**, Shono discloses all claimed subject matter, note;
a) generating a random number, is met by random number generator 24, fig.4;

b) combining the random number with a pixel value, is met by the adder 22, fig.4; (see also fig. 6)

Considering claim **66**, Shono discloses all claimed subject matter, note

a) generating a first random number, is met by the random number generator 24, fig.4;

b) adding the first random number to a first pixel value, is met by the adder 22 that adds the B_L value to the f_H higher order bit pixel value.

c) generating a second random number, is inherently met by the random number generator 24, fig.4 which would continually generate random numbers as desired.

d) adding the second random number to a second pixel value, is met by the adder 22 that adds the B_L value to the f_H higher order bit pixel value.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **4, 6, 7, 48, 67,70** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Shono** (U.S. 5,436,736).

Considering claim **4**, the image processing circuit of claim 1 wherein the threshold value is within a range of approximately 50 - 80.

Regarding claim 4, Shono does not specifically disclose the threshold value to be within a range of approximately 50-80. However, it would have been obvious matter of design choice to modify the Shono reference by having the desired range of threshold values, since applicant has not disclosed having a particular range of approximately 50-80 solves any stated problem.

Considering claim **6**, the image processing circuit of claim 1 wherein the compensation value comprises a randomly generated value within a range of -3 - 3.

Regarding claim 6, see rejection of claim 4;

Considering claim **7**, the image processing circuit of claim 1 wherein the pixel circuit is further operable to: determine whether the sum of the pixel and compensation values is within a predetermined range of pixel values; and set the pixel value equal to a value within the range if the sum is outside of the range.

See rejection of claim 4;

Considering claim **48**, the method of claim 50, further comprising: determining whether the sum of the pixel and compensation values is within a predetermined range of pixel values; and setting the pixel value equal to a value within the range if the sum is outside of the range.

See rejection of claim 4;

Regarding claim **67**, see rejection of claim 35.

Considering claim **70**, the method of claim 66 wherein: the first pixel value corresponds to a starting pixel location in a first video frame; the second pixel value corresponds to the pixel location in a second video frame; and the generating the second random number comprises generating the second random number unequal to the first random number, is implied because if the second random number is equal to the first random number, then the system is repeating the operation it performed earlier and that would be an unacceptable (i.e. inefficient and/or wasteful, etc.) way of processing.

Response to Arguments

5. Applicant's arguments filed 8/24/04 have been fully considered but they are not persuasive. Applicant argues that claims 1 and 45 each recite modifying a pixel value only [newly added limitation, which adds not much at all to the claim] if the pixel value has a predetermined relationship to a threshold value; that Shono unconditionally adds the entirety of the lower-order data to higher-order bit data; and that there is no teaching or suggestion in Shono that modification of the lower-order data is contingent on any relationship or other condition, such as only if the pixel value has a predetermined relationship to the threshold value.

The examiner submits Shono's reference meets the claims as claimed because the comparator compares the pixel data to the threshold value. Shono on col. 5, lines 55-66 teaches the following:

> *"In FIG. 4, a random number generator 24 generates a random number. An operator 25 divides the input pixel data into higher-order bit data f_H and lower-order bit data f_L and sends the higher-order bit data f_H to the adder 22; the lower-order bit data f_L to a comparator 23. The comparator 23 compares a threshold value output from the random number generator 24 with the lower-order bit data f_L and binarizes the lower-order bit data in accordance with the comparison result. The adder 22 adds the higher-order bit data f_H to the binarized data B_L. The output from the adder 22 is h in the equation (1)."* [emphasis added by examiner]

The comparator 23 outputs the result (B_L) of the comparison operation. As mentioned in the rejection above, the latter is not a simple addition or summation of the two values; rather, it is a result of a comparison. The circuit, as Shono also makes it clear on col. 8, lines 20-22, binarizes the lower bit pixel data into 1 or 0 (notice the alternative "or" here) with the random number as a threshold. By definition a threshold is a level, point, or value above which something is true or will take place and below which it is not or will not. (Webster's 10th edition). Shono is taking the lower side of the pixel value which has a relationship to the threshold value, i.e. the threshold value being a predetermined value (see col. 7, lines 42-47), and generates the B_L as a control signal in order to modify the pixel value in the adder 22. As to the argument that "Shono unconditionally adds the entirety of the lower-order data to higher-order bit data", applicant is arguing something that is not found in the claims, because nowhere in the claim(s) is calling for

the value F_l and F_h to be separately compared and modified; rather, the claims recite the "pixel value" in general. Therefore, the reference of Shono meets the claims as claimed because by definition threshold values are predetermined values and the pixel value has a certain relationship to the threshold value, and both the comparator and adder are acting upon the pixel value as a function of the threshold value or vice-versa. Applicant's arguments therefore are unpersuasive and this office action has been made final.

Allowable Subject Matter

6. Claims **15-33 and 39-44,** and **54-65** are allowable over the prior art.

7. Claims **8,12-13, 35-38,46,47,49 52-53, 68-69** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose image processing circuit, wherein the pixel circuit is operable to: a pixel circuit operable to compare a first pixel value to a first threshold value, the first pixel value corresponding to a pixel location in a first video frame, add a first compensation value to the first pixel value if the first pixel value is less than the first threshold value, compare a second pixel value to a second threshold value, the second pixel value corresponding to the pixel location in a second video frame, add a second compensation value to the second pixel value if the second pixel value is less than the second threshold value, as in claims **15** and **54**; a pixel circuit operable to generate a

first random number using a first seed number, compare a first pixel values to a first threshold value, add the first random number to the first pixel value if the first pixel value is less than the first threshold value, generate a second random number using a second seed number, compare a second pixel value to a second threshold value, and add the second random number to the second pixel value if the second pixel value is less than the second threshold value, as in claims **24 and 58**; *truncate* the first random number before adding the first random number to the first pixel value; *truncate* the second random number before adding the second random number to the second pixel value; set the second seed number equal to the *untruncated* first random number, as in claim **28**; wherein generating the first and second random numbers comprises generating the first and second random numbers according to the following equation: random number= (1664525 x seed number+ 1013904223)mod 2^{32}, as in claims **29** and **62**; a pixel circuit operable to, generate a first random number using a first seed number, compare a first pixel value to a first threshold value, the first pixel value corresponding to a starting pixel location in a first video frame, add the first random number to the first pixel value if the first pixel value is less than the first threshold value, generate a second random number using a second seed number, compare a second pixel value to a second threshold value, the second pixel value corresponding to a starting pixel location in a second video frame, add the second random number to the second pixel value if the second pixel value is less than the second threshold value, as in claim **31**; a comparator having a pixel-value input terminal and first and second pixel-value output terminals; a random-number generator having a seed input terminal and a

random-number output terminal; a combiner having a first input terminal coupled to the first pixel-value output terminal, a second input terminal coupled to the random-number output terminal, and a combiner output terminal; and an image buffer having a first input terminal coupled to the second pixel-value output terminal and having a second input terminal coupled to the combiner output terminal, as in claim **39**; and, generating a first random number using a first seed number; comparing a first pixel value to a first threshold value, the first pixel value corresponding to a starting pixel location in a first video frame; adding the first random number to the first pixel value if the first pixel value is less than the first threshold value; generating a second random number using a second seed number; comparing a second pixel value to a second threshold value, the second pixel value corresponding to a starting pixel location in a second video frame; adding the second random number to the second pixel value if the second pixel value is less than the second threshold value, as in claim **63.**

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
March 10, 2005

PAULOS M. NATNAEL
PATENT EXAMINER